In the Claims:

Please add claims 21-26. The claims are as follows:

1-7. (Canceled)

8. (Original) A transistor comprising:

a semiconductor wafer comprising a semiconductor layer overlying a buried insulator having at least two layers;

a first recess and a second recess formed through the semiconductor layer and a first layer of the buried insulator;

a body formed from the semiconductor layer situated between the first recess and the second recess, the body comprising a top body surface and a bottom body surface that define a body thickness;

a source structure formed into the first recess, the source structure comprising a source region; and

a drain structure formed into the second recess, the drain structure comprising a drain region;

wherein a top portion of the source structure and a top portion of the drain structure are within and abut the body thickness.

9. (Original) The transistor of claim 8, wherein the first layer of the buried insulator is at least as thick as the semiconductor layer.

10. (Original) The transistor of claim 8, wherein the semiconductor layer comprises single crystal silicon.

11. (Original) The transistor of claim 8, wherein the buried insulator comprises three layers, wherein a second layer is different from the first layer and a third layer.

12. (Original) The transistor of claim 11, wherein the first layer comprises silicon dioxide, wherein the second layer comprises silicon nitride, wherein the third layer comprises silicon dioxide.

13. (Original) The transistor of claim 8, wherein the first recess and the second recess stop on a second layer of the buried insulator.

14. (Previously presented) The transistor of claim 8, wherein the body comprises a fin structure that comprises a top fin structure surface and a bottom fin structure surface that define a fin structure thickness, wherein the top portion of the source structure and the top portion of the drain structure are below said top fin structure surface, and wherein said source structure and said drain structure abut the fin structure.

15. (Previously presented) A semiconductor wafer comprising a silicon layer on a buried insulator that comprises a first buried insulator layer on a second buried insulator layer different from the first buried insulator layer, a first recess and a second recess formed through the

semiconductor layer and said first buried insulator layer, a body formed from the semiconductor layer situated between the first recess and the second recess, the body comprising a top body surface and a bottom body surface that define a body thickness, wherein the first buried insulator layer is at least as thick as the silicon layer.

16. (Original) The semiconductor wafer of claim 15, wherein the first buried insulator layer comprises silicon dioxide.

17. (Original) The semiconductor wafer of claim 15, wherein the second buried insulator layer comprises silicon nitride.

18. (Original) The semiconductor wafer of claim 15, further comprising a transistor.

19. (Previously presented) The semiconductor wafer of claim 18, wherein the transistor comprises a source structure and a drain structure in said first recess and said second recess, respectively.

20. (Original) The semiconductor wafer of claim 18, wherein the transistor further comprises a fin structure.

21. (New) The transistor of claim 8, wherein a first portion of the buried insulator is disposed between the first recess and the second recess.

22. (New) The transistor of claim 8, wherein the first recess is disposed between a first portion of the buried insulator and a second portion of the buried insulator, and wherein the second recess is disposed between the first portion of the buried insulator and a third portion of the buried insulator.

23. (New) The transistor of claim 8, wherein the semiconductor layer is in direct mechanical contact with a gate dielectric layer at a surface of the gate dielectric layer, wherein the gate dielectric layer is in direct mechanical contact with a gate conductor layer, wherein the semiconductor layer is in direct mechanical contact with the buried insulator at a surface of the buried insulator, and wherein the surface of the gate dielectric layer is about parallel to the surface of the buried insulator.

24. (New) The semiconductor wafer of claim 15, wherein a portion of the first buried insulator layer is disposed between the first recess and the second recess.

25. (New) The semiconductor wafer of claim 15, wherein the first recess is disposed between a first portion of the first buried insulator layer and a second portion of the first buried insulator layer, and wherein the second recess is disposed between the first portion of the first buried insulator layer and a third portion of the first buried insulator layer.

26. (New) The semiconductor wafer of claim 15, wherein the silicon layer is in direct mechanical contact with a gate dielectric layer at a surface of the gate dielectric layer, wherein the gate

dielectric layer is in direct mechanical contact with a gate conductor layer, wherein the silicon layer is in direct mechanical contact with the buried insulator at a surface of the first buried insulator layer, and wherein the surface of the gate dielectric layer is about parallel to the surface of the first buried insulator layer.